AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A stacked semiconductor package comprising a substrate having first and second surfaces opposite to each other, and first and second semiconductor chips each of which has a mounting surface provided with a plurality of chip pins arranged in a predetermined pattern, the first and the second semiconductor chips being mounted on the first and the second surfaces of the substrate, respectively, so that the mounting surfaces are faced to each other with the substrate interposed there between;

wherein the substrate has a plurality of package pins corresponding to the chip pins, respectively, and formed on the first or the second surface in an area different from a chip mounting area where the first or the second semiconductor chip is mounted; and

wherein the package pins are arranged in a pattern identical to the predetermined pattern.

2. - 3. (canceled).

4. (withdrawn): A stacked semiconductor package according to claim 1, wherein the package pins include an option pin connected to a corresponding chip pin of either one of the first and the second semiconductor chips and a regular pin connected to a corresponding chip pin of each of the first and the second semiconductor chips.

5. (withdrawn): A stacked semiconductor package according to claim 4, wherein:

the substrate has a common wire having one end connected to the regular pin and a branch wire portion connecting the other end of the common wire to two chip pins as the corresponding chip pins of the first and the second semiconductor chips;

the wiring length from the one end of the common wire to one of the corresponding chip pins being substantially equal to that from the one end of the common wire to the other of the corresponding chip pins.

6. (withdrawn): A stacked semiconductor package according to claim 5, wherein:

the branch wire portion comprises a via formed in the vicinity of an intermediate position between the two chip pins and connected to the other end of the common wire, and first and second branch wires which are substantially equal to each other in length and which connect the via to the two chip pins.

7. (withdrawn): A stacked semiconductor package according to claim 5, wherein the two chip pins corresponding to the regular pin are faced to each other through the substrate, the branch wire portion has a via directly connecting the two chip pins.

8. (withdrawn): A stacked semiconductor package according to claim 1, wherein the substrate is a multilayer substrate having a ground plane and/or a power supply plane, the

common wire and the branch wire portion each forming a transmission line together with the ground plane and/or the power supply plane.

9. (withdrawn): A stacked semiconductor package according to claim 8, wherein the transmission line comprises any one of a microstrip line, a strip line, and a parallel line.

10. (withdrawn): A stacked semiconductor package according to claim 9, wherein the ground plane and/or the power supply plane includes a portion formed by a plurality of ground plane parts and/or power supply plane parts or a portion partially separated by a via or another wire.

11. (withdrawn): A stacked semiconductor package according to claim 1, wherein the semiconductor chip is an elemental chip (bare die), a chip having a packaged structure obtained by mounting the elemental chip on a substrate, electrically connecting wires (pads) of the elemental chip and wires on the substrate by wire bonding, inner lead bonding, flip-chip connection, or the like, and encapsulating the chip and the substrate in a resin mold in order to protect a conductive pattern on the substrate, or a wafer level CSP or wafer process package.

12. (canceled).

13. (currently amended): A stacked semiconductor package according to claim 1~~claim 12~~, wherein the package pins comprise pins arranged according to the predetermined pattern and additional pins.

14. (currently amended): A stacked semiconductor package according to claim 1, wherein the chip pins of the first semiconductor chip are arranged on the substrate so as to be a mirror-image of the chip pins of the second semiconductor ~~package~~chip.

15. (previously presented): A stacked semiconductor package according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are aligned with one another.

16. (previously presented): A stacked semiconductor package according to claim 1, wherein the chip pins of the first semiconductor chip and the chip pins of the second semiconductor chip are aligned with one another.